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# EXHIBIT Q

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# IEEE Standard Dictionary of Electrical and Electronics Terms

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**actuator, centrifugal (rotating machinery).** Rotor-mounted element of a centrifugal starting switch. *See:* **centrifugal starting switch.** 63

**actuator, relay.** *See:* **relay actuator.**

**actuator valve.** An electropneumatic valve used to control the operation of a brake valve actuator. 328

**acyclic machine (homopolar machine*) (unipolar machine*) (rotating machinery).** A direct-current machine in which the voltage generated in the active conductors maintains the same direction with respect to those conductors.

*Deprecated. 63

**adaptability (software).** The ease with which software allows differing system constraints and user needs to be satisfied. *See:* **software; system.** 434

**adaptation (illuminating engineering).** The process by which the retina becomes accustomed to more or less light than it was exposed to during an immediately preceding period. It results in a change in the sensitivity to light. *Note:* Adaptation is also used to refer to the final state of the process, as reaching a condition of adaptation to this or that level of luminance. *See:* **scotopic vision; photopic vision; chromatic adaptation.** 167

**adapter (1) (general).** A device for connecting parts that will not mate. An accessory to convert a device to a new or modified use. 185

**(2) (test, measurement and diagnostic equipment).** A device or series of devices designed to provide a compatible connection between the unit under test and the test equipment. May include proper stimuli or loads not contained in the test equipment. *See:* **interface.** 54

**adapter kit (test, measurement and diagnostic equipment).** A kit containing an assortment of cables and adapters for use with test or support equipment. 54

**adapter, standard.** A two-port device having standard connectors for joining together two waveguides or transmission lines with nonmating standard connectors. 110

**adapter, waveguide (waveguide components).** A structure used to interconnect two waveguides which differ in size or type. If the modes of propagation also differ, the adapter functions as a mode transducer. 166

**adapting.** *See:* **self-adapting.**

**adaptive antenna system.** An antenna system having circuit elements associated with its radiating elements such that some of the antenna properties are controlled by the received signal. *See:* **antenna.** 111

**adaptive color shift (illuminating engineering).** The change in the perceived object color caused solely by change of the state of chromatic adaptation. *See:* **state of chromatic adaptation.** 167

**adaptive control system.** *See:* **control system, adaptive.**

**adaptive equalization (data transmission).** A system that has a means of monitoring its own frequency response characteristics and a means of varying its own parameters by closed-loop action to obtain the desired overall frequency response. 59

**adaptive maintenance (software).** Maintenance performed to make a software product usable in a changed environment. *See:* **maintenance; software product.** 434

**adaptive system.** A system that has a means of monitoring its own performance and a means of varying its own parameters by closed-loop action to improve its performance. *See:* **system science.** 209

**Adcock antenna.** A pair of vertical antennas separated by a distance of one-half wavelength or less, and connected in phase opposition to produce a radiation pattern having the shape of the figure eight in all planes containing the centers of the two antennas. *See:* **antenna.** 111

**adder.** A device whose output is a representation of the sum of the two or more quantities represented by the inputs. *See:* **half-adder; electronic analog computer.** 235, 54

**addition agent (electroplating).** A substance that, when added to an electrolyte, produces a desired change in the structure or properties of an electrodeposit, without producing any appreciable change in the conductivity of the electrolytes, or in the activity of the metal ions or hydrogen ions. *See:* **electroplating.** 328

**additive (insulating oil).** A chemical compound or compounds added to an insulating fluid for the purpose of imparting new properties or altering those properties which the fluid already has. 461

**address (A) (1) (semiconductor memory).** Those inputs whose states select a particular cell or group of cells. 441

**(2) (electronic computations and data processing).** (A) An identification, as represented by a name, label, or number, for a register, location in storage, or any other data source or destination such as the location of a station in a communication network. (B) Loosely, any part of an instruction that specifies the location of an operand for the instruction. (C) (electronic machine-control system). A means of identifying information or a location in a control system. *Example:* The *x* in the command *x* 12345 is an address identifying the numbers 12345 as referring to a position on the *x* axis. 255

**(3) (software).** (A) A character or group of characters that identifies a register, a particular part of storage, or some other data source or destination. (B) To refer to a device or an item of data. *See:* **data.** 434

**(4) (test pattern language).** The identification of a specific memory word, usually expressed in X-, Y-, and Z-coordinates, and in binary code. *See:* **logic address; physical address.** 463

**address cycle (FASTBUS acquisition and control).** *Syn:* **primary address cycle.** 480

**address, effective (computing systems).** The address that is derived by applying any specified rules (such as rules relating to an index register or indirect address) to the specified address and that is actually used to identify the current operand. 77

**address fields (DSAP [destination service access point] and SSAP [source service access point] )(logical link control).** The ordered pair of service access point addresses at the beginning of an LLC PDU (logical link control protocol data unit) which identifies the LLC(s) designated to receive the PDU and the LLC sending the PDU. Each address field is one octet in length. 585

**address format (computing machines).** The arrangement of the address parts of an instruction. *Note:* The expression plus-one is frequently used to indicate that one of the addresses specifies the location of the next instruction to be executed, such as one-plus-one, two-plus-one, three-plus-one, four-plus-one. 255, 77

**addressing mode (microprocessor assembly language).** The manner in which an operand is to be accessed during execution of an instruction. 466

**address locked operation (FASTBUS acquisition and control).** An operation directed to a single primary address containing a mixture of read and write cycles, possibly including block transfers as well. 480

**address part.** A part of an instruction that usually is an address, but that may be used in some instructions for another purpose. *See:* **instruction code.** 235

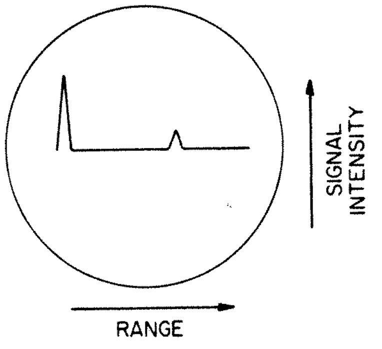
**address register (computing machines).** A register in which an address is stored. 255, 77

**address space (software).** The range of addresses available to a computer program. *See:* **addresses; computer program.** 434

**address, tag.** *See:* **symbolic address.**

**ADF.** *See:* **automatic direction finder.**

**A-display (radar).** A display in which targets appear as vertical deflections from a horizontal line representing a time base. Target distance is indicated by the horizontal position of the deflection from one end of the time base. The amplitude of the vertical deflection is a function of the signal intensity. 13



**A-Display**

**adjacent channel (data transmission).** The channel whose frequency is adjacent to that of the reference channel. 59

**adjacent-channel attenuation (receivers).** *See:* **selectance.**

**adjacent channel interference (data transmission).** Interference, in a reference channel, caused by the operation of an adjacent channel. 59

**adjacent-channel selectivity and desensitization (receiver performance) (receiver).** A measure of the ability to discriminate against a signal at the frequency of the adjacent channel. Desensitization occurs when the level of any off-frequency signal is great enough to alter the useable sensitivity. *See:* **receiver performance.** 181

**adjoint system.** (1) A method of computation based on the reciprocal relation between a system of ordinary linear differential equation and its adjoint. *Note:* By solution of the adjoint system it is possible to obtain the weighting function (response to a unit impulse) $W(T, t)$ of the original system for fixed $T$ (the time of observation) as a function of $t$ (the time of application of the impulse). Thus, this method has particular application to the study of systems with time-varying coefficients. The weighting function then may be used in convolution to give the response of the original system to an arbitrary input. *See:* **electronic analog computer.** 9

(2) For a system whose state equations are $dx(t)/dt = f(x(t),u(t),t)$, the adjoint system is defined as that system whose state equations are $dy(t)/dt = -y(t)$, where $A^*$ is the conjugate transpose of the matrix whose $i,j$ element is $\partial f_i/\partial x_j$. *See:* **control system.** 198

**adjust (instrument).** Change the value of some element of the mechanism, or the circuit of the instrument or of an auxiliary device, to bring the indication to a desired value, within a specified tolerance for a particular value of the quantity measured. *See:* **instrument.** 328

**adjustable (National Electric Code).** (As applied to circuit breakers.) A qualifying term indicating that the circuit breaker can be set to trip at various values of current and/or time within a pre-determined range. 256

**adjustable constant-speed motor.** A motor, the speed of which can be adjusted to any value in the specified range, but when once adjusted the variation of speed with load is a small percentage of that speed. For example, a direct-current shunt motor with field-resistance control designed for a specified range of speed adjustment. *See:* **asynchronous machine.** 63

**adjustable impedance-type ballast (illuminating engineering).** A reference ballast consisting of an adjustable inductive reactor and a suitable adjustable resistor in series. These two components are usually designed so that the resulting combination has sufficient current-carrying capacity and range of impedance to be used with a number of different sizes of lamps. The impedance and power factor of the reactor-resistor combination are adjusted and checked each time the unit is used. 271

**adjustable-speed drive (industrial control).** An electric drive designed to provide easily operable means for speed adjustment of the motor, within a specified speed range. *See:* **electric drive.** 206

**adjustable-speed motor.** A motor the speed of which

# EXHIBIT R

# DICTIONARY OF
# COMPUTING

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**adaptive maintenance** *See* software maintenance.

**adaptive process** The process of performing computations on a set of measured or presented data (believed to be) from a physical, i.e. natural, source in such a way as to develop a "best" parametric model of that physical source, i.e. one that best fits the observed data according to some error criterion. *See also* adaptive-control system, self-organizing system.

**adaptive quadrature** *See* numerical integration.

**ADC** *Abbrev. for* analog-to-digital (A/D) converter.

**ADCCP** *Abbrev. for* advanced data communication control procedure. A bit-oriented *data link control protocol developed by ANSI and similar to *SDLC and *HDLC.

**A/D converter (ADC)** *Short for* analog-to-digital converter. A device that can accept an analog, i.e. continuous, signal whose amplitude lies within a given range, and produce an equivalent digital signal, i.e. an *n*-bit parallel binary word that represents this analog signal. The analog signal is "examined" at discrete fixed intervals of time by means of a *sampling process in order to produce the digital signal. Analog signals originating from devices such as analog sensors or tachogenerators may thus be converted into a form that can then be processed by, say, a microprocessor.

The *resolution* of an A/D converter gives the smallest change in analog input that can be discriminated by the device. If the voltage range of an *n*-bit A/D converter is *V*, then its resolution is

$$V(2^n - 1)$$

Since the resolution is finite, the conversion process introduces quantization noise (*see* discrete and continuous systems). A/D converters are available in integrated circuit form. *See also* D/A converter.

**adder** In its simplest form, a digital electronic device that performs the operation of addition on two binary digits, the *augend* and the number to be added, the *addend*. It is therefore also known as a *binary adder*. This operation is exemplified by the truth table shown in Fig. *a*, where $\Sigma$ is the sum and $C_0$ is the carry. From this it can be seen that binary addition may generate a carry to subsequent stages.

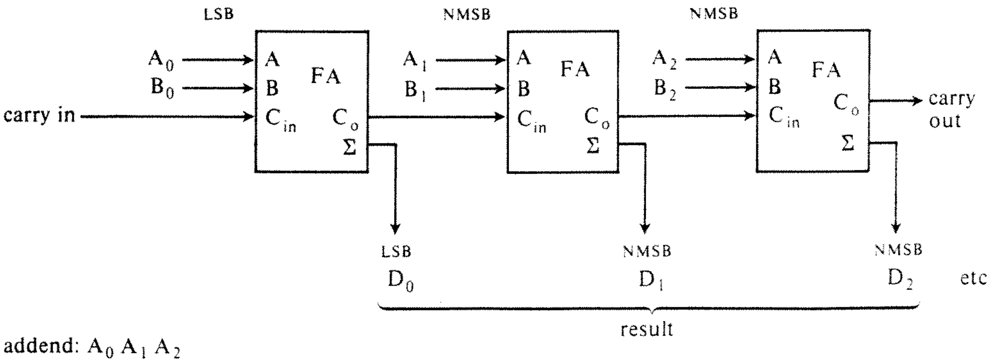
A *full adder* has provision for inputs of addend, augend, and carry bits and is capable of generating sum and carry outputs. These adders may be cascaded when it is desired to add binary words greater than one bit in length by connecting together the carry inputs and outputs of adjacent stages. The circuit shown in Fig. *b* is a *parallel adder operating on two 3-bit binary words ($A_0A_1A_2$ and $B_0B_1B_2$) to produce a 3-bit result ($D_0D_1D_2$) and a carry. The adder uses a *ripple-carry* technique: the carry at each stage of addition must propagate or ripple through the succeeding stages of addition in order to form the result.

A *half-adder* is an implementation of an adder that has provision only for input of addend and augend bits and is capable of generating sum and carry outputs. These devices cannot directly be cascaded as can full adders but may be made to perform a similar function by including additional logic gating, as shown in Fig. *c*. This type of adder is relatively slow in operation. *See also* BCD adder, serial adder, carry lookahead.

**address 1.** The term most generally used to refer (in some way) to a location within the computer memory; the word *location* is actually used as a synonym. Such reference is usually made for the purpose of retrieving or storing some information at that location. The refer-

| A | B | Σ | $C_o$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Fig. *a* Truth table of binary addition


LSB
NMSB
NMSB
$A_0$
$B_0$
carry in
A
B
$C_{in}$
FA
$C_o$
Σ
$A_1$
$B_1$
$A_2$
$B_2$
carry out
LSB
$D_0$
NMSB
$D_1$
NMSB
$D_2$
etc
result

addend: $A_0\ A_1\ A_2$
augend: $B_0\ B_1\ B_2$
result: $D_0\ D_1\ D_2$

LSB : least significant bit
NMSB : next most significant bit

Fig. *b* Parallel 3-bit ripple-carry adder using cascaded full adders

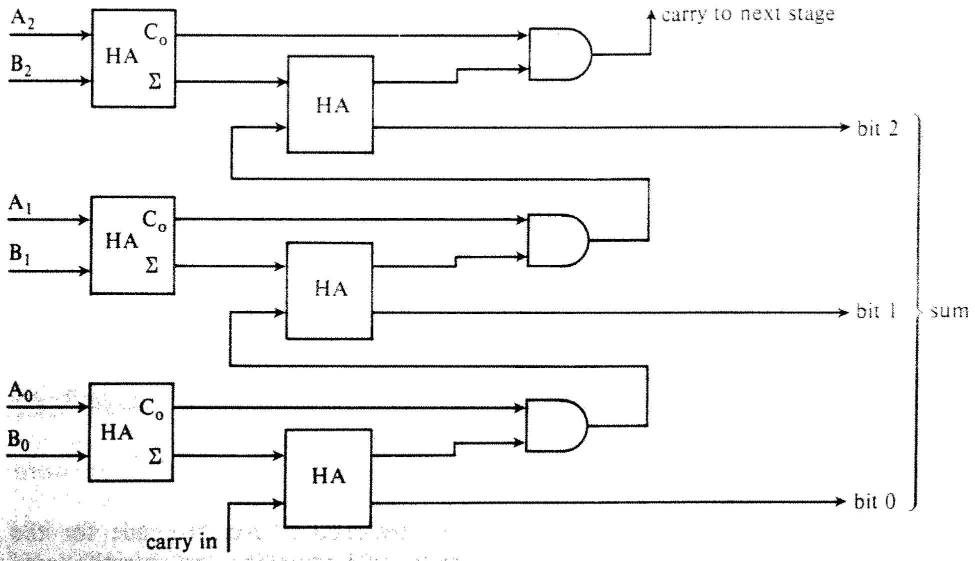

$A_2$
$B_2$
HA
$C_o$
Σ
carry to next stage
bit 2
$A_1$
$B_1$
bit 1
sum
$A_0$
$B_0$
bit 0
carry in

**Fig. *c* Parallel 3-bit ripple-carry adder using half adders and additional gating**

ence may be explicit (*see* direct addressing) or it may be made in any of a number of ways for convenience or brevity (*see* addressing schemes). In some architectures the registers in the CPU and/or the I/O devices are also addressed.

The word address is also used as a verb: to specify a location.

**2.** In communications, *see* addressing.

**addressable location** A location whose position in a storage medium is precisely defined and can be accessed. As a safeguard it is usual to arrange that not all memory locations are addressable by all programs.

**address bus** A *bus that is dedicated to passing address information. It may be a set of conductors that are physically separate from other dedicated buses or it may be a subset of a system bus. The number of conductors is often the same as the maximum allowable number of bits in the address.

**address calculation sorting** A form of *sorting that uses extra storage space to improve upon a *straight insertion sort. One method employs *n* *list heads, corresponding to *n* different ranges of the sortkey, together with a *link field on each record.

**address format** *See* instruction format.

**addressing** The method used to identify the location of a participant in a *network. Ideally, addressing specifies where the participant is located rather than who they are (*see* name) or how to get there (*see* routing). This is true for *flat addressing*, in which addresses are assigned independently of each other and carry no internal structure. More common, however, is *hierarchical addressing*, in which addresses are grouped to reflect relationships among the addressed entities. Often the grouping reflects the physical topology of the network, so addressing and routing are interrelated. Sometimes the grouping reflects administrative or functional relationships (*logical addressing*), so addressing and naming are interrelated.

In a system employing layered protocols (*see* X.25, seven-layer reference model), different forms of addressing may be used at different levels. The data link level may use addresses that identify specific stations on a multidrop line. The network level uses addresses that identify the source and destination hosts associated with a packet. Higher protocol layers may use addresses that distinguish different connections or processes.

Addresses may be fixed-length or extensible. In *fixed-length addressing* all addresses occupy a fixed number of digits. An example is the Ethernet protocol, which uses 48-bit addresses. In *extensible addressing* the length of an address may vary from case to case. For example, in *X.121 "international data numbers" are defined and these may be from 3 to 14 decimal digits in length.

**addressing schemes** The wide variety of schemes developed in order to provide compact or convenient *address references in cases where the *absolute address is too large to be comfortably included in an instruction (*see* instruction format) or where it is not possible or even necessary to assign an explicit address. *Augmented, *indirect, *implied, *immediate, and *relative addressing schemes provide compact references. *Indexed, relative, and *symbolic addressing schemes provide convenient references. In the absence of any of these addressing schemes *direct addressing is used.

**address mapping** Use of one of the *addressing schemes to convert an address that is specified in an instruction into an *absolute address. *Virtual memory and *cache memory use forms of address mapping for additional memory-management functions.

**address mark** The special code or d.c.-erased area on a magnetic disk track that occurs just prior to the address information of a *sector. In the case of an MFM drive using a special code (*see* disk format), the encoding rules for MFM are broken so that the code is unique. The purpose of the address mark is to bring the drive control electronics into byte synchronization.

The *data mark* fulfills the same function with respect to data as the address mark to the address.

**address register** A *register in which an *address is stored. *See also* control unit.

**address-relative** Having or involving a relative address or relative addresses. *See* relative addressing.

**address space** The number of distinct locations that may be referred to with the *absolute address. For most (i.e. binary) machines it is equal to $2^n$, where $n$ is the number of bits in the absolute address. In many large machines the address space is larger than the number of physical or real addresses that are present in the system. Additionally, the number of bits available to specify an address is restricted (*see* instruction format), and some form of *address mapping or *addressing scheme is used to obtain the absolute address from the specified address. The address space embraces the primary memory, the I/O devices, and, in some cases, the registers in the CPU.

**address table sorting** A form of *sorting that is useful when the information records are long. A table of addresses that point to the records is formed and these addresses, rather than the records themselves, are manipulated.

**add-subtract time** The time required by a computer to find the sum or difference of two numbers; it may or may not include the time required to obtain the numbers from memory. This is often used as one form of (speed) figure of merit for computers. *See also* computer power.

**adjacency list** *Another name for* adjacency structure.

**adjacency matrix (connectivity matrix; reachability matrix)** A *matrix used as a means of representing a *graph. If $A$ is the adjacency matrix corresponding to a given graph $G$, then

$$a_{ij} = 1$$

if there is an edge from vertex $i$ to vertex $j$ in $G$; otherwise

$$a_{ij} = 0$$

If $G$ is a directed *graph then

$$a_{ij} = 1$$

if there is an edge directed from vertex $i$ to vertex $j$; otherwise

$$a_{ij} = 0$$

If the vertices of the graph are numbered $1,2, \ldots m$, the adjacency matrix is of a type $m \times m$. If

$$A \times A \times \ldots \times A$$
$$(p \text{ terms}, p \leqslant m)$$

is evaluated, the nonzero entries indicate those vertices that are joined by a *path of length $p$; indeed the value of the $i,j$th entry of $A^p$ gives the number of paths of length $p$ from the vertex $i$ to vertex $j$. By examining the set of such matrices,

$$p = 1,2, \ldots, m-1$$

it can be determined whether two vertices are connected.

It is also possible for adjacency matrices to be formed from *Boolean matrices.

**adjacency structure (adjacency list)** A means of representing a *graph. The adjacency structure corresponding to a *path $G$ is the set

$$\{\text{Adj}(v) \mid v \text{ is a vertex in } G\}$$

If $G$ is an undirected graph, then a vertex $w$ is in Adj($v$) if and only if there is an edge in $G$ between $v$ and $w$; if $G$ is a directed graph, then $w$ is in Adj($v$) if and only if there is an edge in $G$ directed from $v$ to $w$.